20 GHz High Power High Efficiency HEMT Module

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Abstract

We are reporting the development of a high gain, high power and high efficiency K-band MIC power module employing four 1.6 mm pseudomorphic InGaAs HEMT devices. Power output of 3.2 Watts with 10 dB gain and 35% power-added efficiency at 3 dB compression was obtained at 20 GHz. The 1 dB bandwidth is 1.7 GHz.

Introduction

There is a growing interest in using 20 GHz solid state power amplifiers (SSPA) for spacecraft on-board power amplifier applications to take advantages of an SSPA approach. Power amplifiers with output power of up to 12 watts with an efficiency of 15.5% have been demonstrated using GaAs MESFET devices at this frequency (ref. 1, 2). However, the power performance of large MESFET devices degrade, especially in power gain and efficiency, as the operating frequencies go be d 18 GHz. For example, while 1-watt level power HEMT is capable of around 10 dB power gain at more than 30% power-added efficiency (PAE) at 20 GHz, it becomes more difficult for a comparable MESFET to achieve > 6 dB power gain and >30% PAE at the same frequency (ref. 1).

AlGaAs/InGaAs pseudomorphic HEMTs, on the other hand, have demonstrated superior simultaneous power, gain and power-added efficiency at both microwave and millimeter-wave frequencies (ref. 3) and they are considered as the most viable device technology for this application. This paper presents the development of a high gain and high efficiency one-stage PHEMT power module which has demonstrated 3.2 W power output, 10 dB saturated gain and 35% power-added efficiency at 20 GHz with a 1 dB bandwidth of 1.7 GHz. The availability of such high performance power modules should greatly facilitate the development of low cost high performance SSPAs capable of tens of Watt power output at K-band.

Device Design and Characteristics

The power HEMT design was optimized for high current and high operating voltage to achieve maximum power output. The device structure is a planar-doped AlGaAs/InGaAs double heterostructure pseudomorphic HEMT whose cross section is shown in Figure 1. Silicon planar dopings were inserted into the AlGaAs insulator and the confinement layers with 20 Å offset from the channel resulting a sheet charge density of 2.9 E12 /cm2 in the channel at 300 °K. The chnnel thickness was kept to below 150 Å to prevent the strained InGaAs layer from being relaxed. This structure is realized with molecular beam epitaxy to achieve precise doping and thickness control and sharp interfaces between different layers for best power performance.

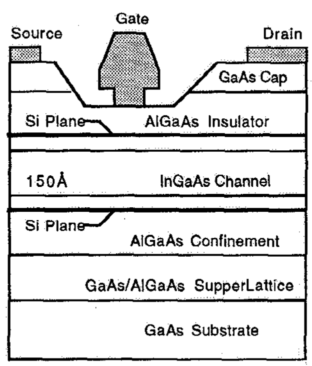

Figure 1 AlGaAs/InGaAs pseudomorphic power HEMT structure.

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The basic power HEMT cell has 1.6 mm gate periphery comprising of 16 gate fingers. Each finger is 0.2 µm in length and 100 µm in width. The layout of this basic cell is shown in Figure 2 and the overall chip size is 0.675 mm x 0.300 mm. High gate to drain diode breakdown (10 to 12 V @ 0.1 mA/mm) was achieved with single gate recess which allowed us to bias the device at 5 to 6 volts for high power and high efficiency. The maximum current density exceeded 450 mA/mm while the drain current and the transconductance were greater than 300 mA/mm and 550 mS/mm respectively. The device cutoff frequency was 55 GHz.

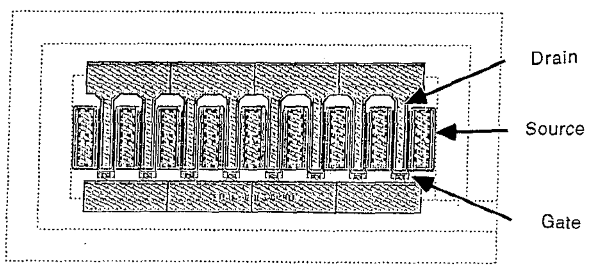

Figure 2 Layout of baseline 1.6 mm power HEMT device.

Power Module Design

The single-stage power module is shown in Figure 3. Figure 3(a) shows the schematic plot of equivalent circuit elements of the matching/bias networks. Figure 3(b) shows the layout of these networks. It consists of four 1600um devices together with matching/combining circuitry and bias and stabilization networks. The four 1600um cells are combined using an in-phase combiner/divider network which simultaneously combines and matches the four devices.

This circuit topology was chosen for simplicity and ease of tuning. Because of the difficulty of realizing reliable low parasitic grounds in hybrid MICs and the difficulty of tuning grounded matching elements, shunt matching elements were purposely avoided in this design. Instead, a design consisting of a cascade of transmission line elements was selected. Specifically, the input network consists of a two-section quarter-wave impedance transformer. This network simultaneously divides the input power and matches the input impedance of the 4-cell array to 50 ohms. Similarly, the output network, composed of a two-section cascade of quarter-wave transmission lines, combines the power of these four devices and provides a large-signal match. The isolation resistors, labeled R1 through R4 in the figure, are selected to terminate the three odd modes this network can supportt.

The bias and bias decoupling networks are also integrated into the module and are designed to be independent of the matching networks. This avoids interaction between the bias and matching networks. As shown in the schematic, the bias network consists of a high impedance quarter-wave transmission line with an open circuit low impedance quarter-wave line serving as an RF short circuit. In addition, two decoupling capacitors (10pF and 0.1uF) are employed in the bias circuit to suppress low frequency oscillations. A stabilizing resistor is also included in the gate bias network to prevent oscillations.

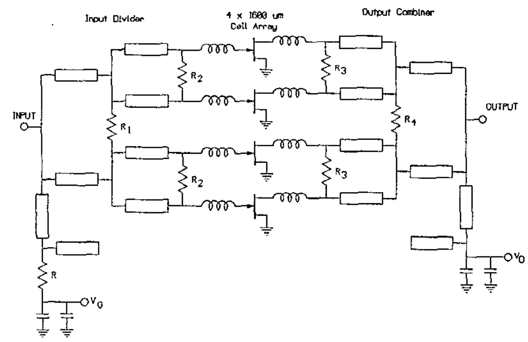

Figure 3 (a) A schematic plot of equivalent circuit elements of the matching/bias network for four-cell HEMTs.

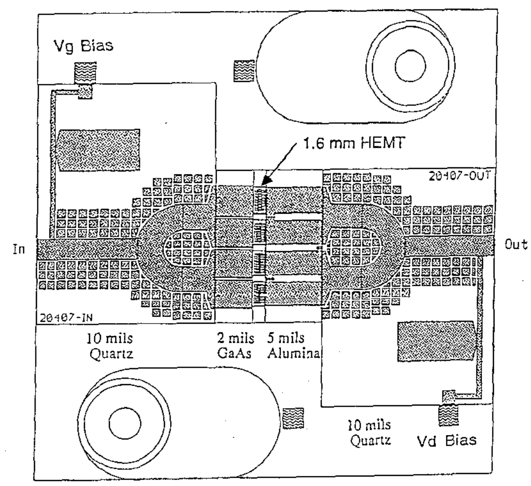

Figure 3(b) Layout of the matching/bias networks for four-cell HEMTs.

This four-cell power HEMT packaged into a 50-ohm microstrip transmission line is shown in Figure 4. Figure 4(a) shows the whole fixture while Figure 4(b) shows the close-up look of the circuit. In order to realize the Zo values required by the divider/combiner, this power module was fabricated with three different substrate materials. The first quarter-wave transformer on the input is contained on a 10 mil thick fused silica substrate. The second quarter-wave transformer is fabricated on 2 mil (50 um) thick GaAs. Similarly, the output circuit is fabricated on 5 mil thick alumina and 10 mil thick fused silica. The overall dimensions of the module, excluding the bias lines, are approximately 450 x 150 mils.

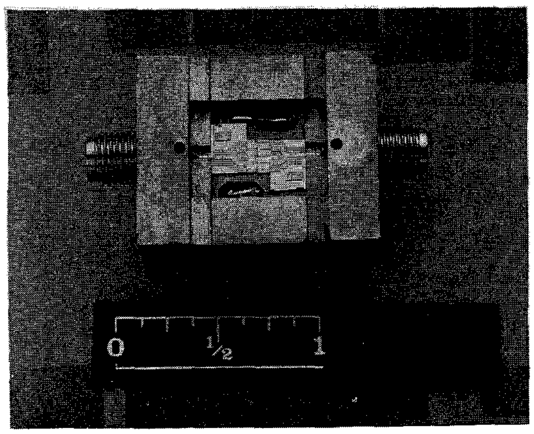

Figure 4(a) Four-cell HEMT fixture.

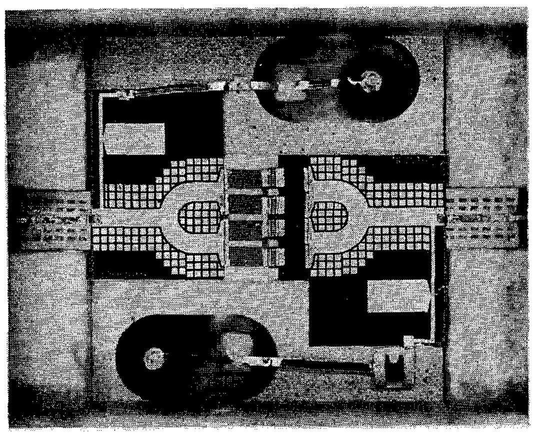

Figure 4(b) The close-up look of the circuit.

HEMT Power Module Performance

We have fabricated power modules employing one, two and four baseline 1.6 mm power HEMT chips. The power output and the power-added efficiency performance for these three types of modules are summarized in Figure 5. For the baseline 1.6 mm power HEMT, 1.0 W power output with 8 dB gain and 32.8% PAE were obtained. The best reported MESFET results that we are aware of are 2 watts output power with 30% PAE and 5 dB gain from a 4.8 mm MESFET with on-chip matching (ref. 1). When normalized with gate width, the power HEMT shows much better capability in saturated gain, efficiency, and power density.

Similarly, 1.6 W power output with 10 dB gain and 36% PAE and 3.2 W power output with 10 dB gain and 35% PAE were achieved with two- and four-chip HEMT modules. All the power HEMTs were operated at class AB. As a comparison, the 3.2 Watt MESFET module reported in reference 1 only has an associated gain of 4.5 dB and 17% PAE. Notice that the performance of the four-chip module scales almost directly with that of the two-chip module. The excellent results obtained from multi-chip modules are attributed to excellent starting HEMT material and chip fabrication process as well as good device-to-device and device-to-circuit matching.

Despite the drawback of the off-chip matching approach undertaken here, the four-chip module still demonstrated a 1-dB bandwidth of 1.7 GHz centered around 20 GHz. The broadband performance is expected to be improved using on-chip matching.

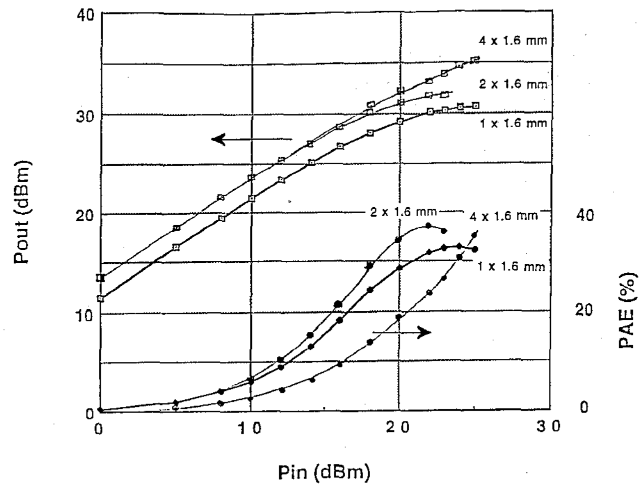

Figure 5 Power output and power-added efficiency of one-, two- and four-chip power modules at 20 GHz.

Conclusions

In this work, we have demonstrated excellent high power and high efficiency performance of pseudomorphic InGaAs HEMTs at 20 GHz. At power output level of one watt or higher, these results of 500 mW/mm power density, 10 dB saturated gain, and greater than 30% PAE from a single device exceed what was reported for the MESFET of comparable sizes. The greatly improved power gain and efficiency offer several design advantages in terms of higher SSPA efficiency, fewer stages and fewer modules required and the attendant improved reliability for the on-board application at 20 GHz.

Acknowledgement

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References

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